JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR
Draft Academic Regulations of M.Tech. (Full Time/Regular) Programme
(Effective for the students admitted into I year from the Academic Year 2021-22 and onwards)

Jawaharlal Nehru Technological University Anantapur (JNTUA) offers **Two** Years (**Four** Semesters) full-time Master of Technology (M.Tech.) Degree programme, under Choice Based Credit System (CBCS) in different branches of Engineering and Technology with different specializations.

The Jawaharlal Nehru Technological University Anantapur shall confer M. Tech. degree on candidates who are admitted to the programme and fulfill all the requirements for the award of the degree.

1. **Award of the M.Tech. Degree**
   A student will be declared eligible for the award of the M.Tech. degree if he/she fulfils the following:
   1.1 Pursues a course of study for not less than two academic years and not more than four academic years.
   1.2 Registers for 70 credits and secures all 70 credits.

2. Students, who fail to fulfil all the academic requirements for the award of the degree within four academic years from the year of their admission, shall forfeit their seat in M.Tech. course and their admission stands cancelled.

3. **Programme of Study:**
   The following M.Tech. Specializations are offered at present in different branches of Engineering and Technology in non-autonomous affiliated colleges:

S.No.	Discipline	Name of the Specialization	Code
01	Civil Engineering	Structural Engineering	20
		Geotechnical Engineering	12
		Computer Aided Structural Engineering	35
		Construction Planning &Management	21
		Structural Engineering &Construction Management	91
		Highway Engineering	93
02	Electrical and Electronics Engineering	Electrical Power Systems	07
		Power Electronics	43
		Power Electronics & Electrical Drives	54
		Power Systems	82
03	Mechanical Engineering	CAD / CAM	04
		Machine Design	15
		Thermal Science & Energy Systems	11
		Refrigeration & Air- Conditioning	17
		Advanced Manufacturing Systems	87

		Thermal Engineering	88
		Production Engineering &Engineering Design	90
		Production Engineering	94
04	Electronics and Communication Engineering	Digital Electronics & Communication Systems	38
		Electronics & Communication Engineering	70
		Digital Systems & Computer Electronics	06
		Embedded Systems	55
		VLSI Design	57
		VLSI System Design	
		VLSI	
		VLSI & Embedded Systems	68
		Embedded Systems & VLSI	
		VLSI and Embedded Systems Design	85
05	Computer Science and Engineering	Computer Science & Engineering	58
		Software Engineering	25
		Computer Networks	08
		Artificial Intelligence & Machine Learning	98

and any other specializations as approved by AICTE/University from time to time.

4. **Eligibility for Admissions**:

4.1 Admission to the M. Tech Program shall be made subject to the eligibility, qualification and specialization prescribed by the A.P. State Government/University from time to time.

4.2 Admissions shall be made either on the basis of either the merit rank or Percentile obtained by the qualified student in the relevant qualifying GATE Examination/ the merit rank obtained by the qualified student in an entrance test conducted by A.P. State Government (APPGECET) for M.Tech. programmes/an entrance test conducted by University/on the basis of any other exams approved by the University, subject to reservations as laid down by the Govt. from time to time.

5. **Programme related terms:**

5.1 ***Credit:*** A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (Lecture/Tutorial) or two hours of practical work/field work per week.

Credit definition:

1 Hr. Lecture (L) per week	1 credit
1 Hr. Tutorial (T) per week	1 credit
1 Hr. Practical (P) per week	0.5 credit

5.2 ***Academic Year:*** Two consecutive (one odd + one even) semesters constitute one academic year.

5.3 ***Choice Based Credit System (CBCS):*** The CBCS provides choice for students to select from the prescribed courses.

6. **Programme Pattern:**

6.1 Total duration of the of M.Tech. programme is two academic years

6.2 Each academic year of study is divided into two semesters.

6.3 Each Semester shall be of 22 weeks duration (inclusive of Examinations), with a minimum of 90 instructional days per semester.

6.4 The student shall not take more than four academic years to fulfill all the academic requirements for the award of M.Tech. degree from the date of commencement of first year first semester, failing which the student shall forfeit the seat in M.Tech. programme.

6.5 The medium of instruction of the programme (including examinations and project reports) will be in English only.

6.6 All subjects/courses offered for the M.Tech. degree programme are broadly classified as follows:

S.No.	Broad Course Classification	Course Category	Description
1.	Core Courses	Foundational & Professional Core Courses (PC)	Includes subjects related to the parent discipline/department/branch of Engineering
2.	Elective Courses	Professional Elective Courses (PE)	Includes elective subjects related to the parent discipline/department/ branch of Engineering
		Open Elective Courses (OE)	Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline which are of importance in the context of special skill development
3.	Research	Research methodology & IPR	To understand importance and process of creation of patents through research
		Technical Seminar	Ensures preparedness of students to undertake major projects/Dissertation, based on core contents related to specialization
		Cocurricular Activities	Attending conferences, scientific presentations and other scholarly activities
		Dissertation	M.Tech. Project or Major Project
4.	Audit Courses	Mandatory noncredit courses	Covering subjects of developing desired attitude among the learners is on the line of initiatives such as Unnat Bharat Abhiyan, Yoga, Value education etc.

6.7 The college shall take measures to implement Virtual Labs (https://www.vlab.co.in) which provide remote access to labs in various disciplines of Engineering and will help student in learning basic and advanced concept through remote experimentation. Student shall be made to work on virtual lab experiments during the regular labs.

6.8 A faculty advisor/mentor shall be assigned to each specialization to advise students on the programme, its Course Structure and Curriculum, Choice of Courses, based on his competence, progress, pre-requisites and interest.

6.9 Preferably 25% course work for the theory courses in every semester shall be conducted in the blended mode of learning.

7. Attendance Requirements:

7.1 A student shall be eligible to appear for the University external examinations if he/she acquires i) a minimum of 50% attendance in each course and ii) 75% of attendance in aggregate of all the courses.

7.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester may be granted by the College Academic Committee.

7.3 Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence

7.4 Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examination of that class.

7.5 A stipulated fee shall be payable towards condonation of shortage of attendance.

7.6 A student will not be promoted to the next semester unless he satisfies the attendance requirements of the present semester. They may seek re-admission into that semester when offered next.

7.7 If any candidate fulfils the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

7.8 If the learning is carried out in blended mode (both offline & online), then the total attendance of the student shall be calculated considering the offline and online attendance of the student.

8. Evaluation – Distribution and Weightage of Marks:

The performance of a student in each semester shall be evaluated subject - wise (irrespective of credits assigned), for a maximum of 100 marks for theory and 100 marks for practical, based on Internal Evaluation and End Semester Examination.

8.1 There shall be five units in each of the theory subjects. For the theory subjects 60 marks will be for the End Examination and 40 marks will be for Internal Evaluation.

8.2 Two Internal Examinations shall be conducted for 30 marks each, one in the middle of the Semester and the other immediately after the completion of instruction. First mid examination shall be conducted for I & II units of the syllabus and second mid examination for III, IV & V units. Each mid exam shall be conducted for a total duration of 120 minutes with 3 questions (without choice) each question for 10 marks. Final Internal marks for a total of 30 marks shall be arrived at by considering the marks secured by the student in both the internal examinations with 80% weightage to the better internal exam and 20% to the other. There shall be an online examination (TWO) conducted during the respective mid examinations by the college for the remaining 10 marks with 20 objective questions.

8.3 The following pattern shall be followed in the End Examination:

i. Five questions shall be set from each of the five units with either/or type for 12 marks each.
ii. All the questions have to be answered compulsorily.
iii. Each question may consist of one, two or more bits.

8.4 For practical subjects, 60 marks shall be for the End Semester Examinations and 40 marks will be for internal evaluation based on the day-to-day performance.

The internal evaluation based on the day-to-day work-10 marks, record- 10 marks and the remaining 20 marks to be awarded by conducting an internal laboratory test. The end examination shall be conducted by the examiners, with a breakup mark of Procedure-10, Experimentation-25, Results-10, Viva-voce-15.

8.5 There shall be a **Technical Seminar** during I year II semester for internal evaluation of 100 marks. A student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, supervisor/mentor and two other faculty members of the department. The student has to secure a minimum of 50% of marks, to be declared successful. If he fails to obtain the minimum marks, he has to reappear for the same as and when supplementary examinations are conducted. The Technical seminar shall be conducted anytime during the semester as per the convenience of the Project Review Committee and students. There shall be no external examination for Technical Seminar.

8.6 There shall be Mandatory **Audit courses** in I & II semesters for zero credits. There is no external examination for audit courses. However, attendance shall be considered while calculating aggregate attendance and student shall be declared to have passed the mandatory course only when he/she secures 50% or more in the internal examinations. In case, the student fails, a re-examination shall be conducted for failed candidates for 40 marks every six months/semester satisfying the conditions mentioned in item 1 & 2 of the regulations.

8.7 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

8.8 In case the candidate does not secure the minimum academic requirement in any of the subjects he/she has to reappear for the Semester Examination either supplementary or regular in that subject or repeat the course when next offered or do any other specified subject as may be required.

8.9 The laboratory records and mid semester test papers shall be preserved for a minimum of 3 years in the respective institutions as per the University norms and shall be produced to the Committees of the University as and when the same are asked for.

9. **Credit Transfer Policy**

As per University Grants Commission (Credit Framework for Online Learning Courses through SWAYAM) Regulation, 2016, the University shall allow up to a maximum of 40% of the total courses being offered in a particular Programme in a semester through the Online Learning courses through SWAYAM.

9.1 The University shall offer credit mobility for MOOCs and give the equivalent credit weightage to the students for the credits earned through online learning courses through SWAYAM platform.

9.2 The online learning courses available on the SWAYAM platform will be considered for credit transfer. SWAYAM course credits are as specified in the platform

9.3 Student registration for the MOOCs shall be only through the institution, it is mandatory for the student to share necessary information with the institution

9.4 The institution shall select the courses to be permitted for credit transfer through SWAYAM. However, while selecting courses in the online platform institution would essentially avoid the courses offered through the curriculum in the offline mode.

9.5 The institution shall notify at the beginning of semester the list of the online learning courses eligible for credit transfer in the forthcoming Semester.

9.6 The institution shall also ensure that the student has to complete the course and produce the course completion certificate as per the academic schedule given for the regular courses in that semester

9.7 The institution shall designate a faculty member as a Mentor for each course to guide the students from registration till completion of the credit course.

9.8 The university shall ensure no overlap of SWAYAM MOOC exams with that of the university examination schedule. In case of delay in SWAYAM results, the university will re-issue the marks sheet for such students.

9.9 Student pursuing courses under MOOCs shall acquire the required credits only after successful completion of the course and submitting a certificate issued by the competent authority along with the percentage of marks and grades.

9.10 The institution shall submit the following to the examination section of the university:

a) List of students who have passed MOOC courses in the current semester along with the certificates of completion.

b) Undertaking form filled by the students for credit transfer.

9.11 The university shall resolve any issues that may arise in the implementation of this policy from time to time and shall review its credit transfer policy in the

light of periodic changes brought by UGC, SWAYAM, NPTEL and state government.

Note: Students shall also be permitted to register for MOOCs offered through online platforms other than SWAYAM NPTEL. In such cases, credit transfer shall be permitted only after seeking approval of the University at least three months prior to the commencement of the semester.

10. **Re-registration for Improvement of Internal Evaluation Marks**:

A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and has failed in the end examination

10.1 The candidate should have completed the course work and obtained examinations results for **I, II and III** semesters.

10.2 The candidate should have passed all the subjects for which the Internal Evaluation marks secured are more than 50%.

10.3 Out of the subjects the candidate has failed in the examination due to Internal Evaluation marks secured being less than 50%, the candidate shall be given one chance for each Theory subject and for a maximum of **three** Theory subjects for Improvement of Internal evaluation marks.

10.4 The candidate has to re-register for the chosen subjects and fulfill the academic requirements.

10.5 For reregistration the candidates have to apply to the University through the college by paying the requisite fees and get approval from the University before the start of the semester in which re-registration is required

10.6 In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

11. Evaluation of Project/Dissertation Work:

The Project work shall be initiated at the beginning of the III Semester and the duration of the Project is of two semesters. Evaluation of Project work is for 300 marks with 200 marks for internal evaluation and 100 marks for external evaluation. Internal evaluation of the Project Work – I & Project work – II in III & IV semesters respectively shall be for 100 marks each. External evaluation of final Project work viva voce in IV semester shall be for 100 marks.

A Project Review Committee (PRC) shall be constituted with the Head of the Department as Chairperson, Project Supervisor and one faculty member of the department offering the M.Tech. programme.

11.1 A candidate is permitted to register for the Project Work in III Semester after satisfying the attendance requirement in all the subjects, both theory and laboratory (in I & II semesters).

11.2 A candidate is permitted to submit Project dissertation with the approval of PRC. The candidate has to pass all the theory, practical and other courses before submission of the Thesis.

11.4 Project work shall be carried out under the supervision of teacher in the parent department concerned.

11.5 A candidate shall be permitted to work on the project in an industry/research organization on the recommendation of the Head of the Department. In such cases,one of the teachers from the department concerned would be the internal guide and an expert from the industry/ research organization concerned shall act as co-supervisor/ external guide. It is mandatory for the candidate to make full disclosure of all data/results on which they wish to base their dissertation. They cannot claim confidentiality simply because it would come into conflict with the Industry's or R&D laboratory's own interests. A certificate from the external supervisor is to be included in the dissertation.

11.6 Continuous assessment of Project Work - I and Project Work – II in III & IV semesters respectively will be monitored by the PRC.

11.7 The candidate shall submit status report by giving seminars in three different phases (two in III semester and one in IV semester) during the project work period. These seminar reports must be approved by the PRC before submission of the Project Thesis.

11.8 After registration, a candidate must present in Project Work Review - I, in consultation with his Project Supervisor, the title, objective and plan of action of his Project work to the PRC for approval within four weeks from the commencement of III Semester. Only after obtaining the approval of the PRC can the student initiate the project work.

11.9 The Project Work Review - II in III semester carries internal marks of 100. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Project Work.

11.10 A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review - II. Only after successful completion of Project Work Review – II, candidate shall be permitted for Project Work Review – III in IV Semester. The unsuccessful students in Project Work Review - II shall reappear for it as and when supplementary examinations are conducted.

11.11 The Project Work Review - III in IV semester carries 100 internal marks. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The PRC will examine the overall progress

of the Project Work and decide whether or not eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review - III. If he fails to obtain the required minimum marks, he has to reappear for Project Work Review - III after a month.

11.12 For the approval of PRC the candidate shall submit the draft copy of dissertation to the Head of the Department and make an oral presentation before the PRC.

11.13 After approval from the PRC, the students are required to submit a report showing that the plagiarism is within 30%. The dissertation report will be accepted only when the plagiarism is within 30%, which shall be submitted along with the dissertation report.

11.14 Research paper related to the Project Work shall be published in conference proceedings/UGC recognized journal. A copy of the published research paper shall be attached to the dissertation.

11.15 After successful plagiarism check and publication of research paper, three copies of the dissertation certified by the supervisor and HOD shall be submitted to the College.

11.16 The dissertation shall be adjudicated by an external examiner selected by the University. For this, the Principal of the College shall submit a panel of three examiners as submitted by the supervisor concerned and department head for each student. However, the dissertation will be adjudicated by one examiner nominated by the University.

11.17 If the report of the examiner is not satisfactory, the candidate shall revise and resubmit the dissertation, in the time frame as decided by the PRC. If report of the examiner is unfavorable again, the thesis shall be summarily rejected. The candidate has to reregister for the project and complete the project within the stipulated time after taking the approval from the University

11.18 If the report of the examiner is satisfactory, the Head of the Department shall coordinate and make arrangements for the conduct of Project Viva voce exam.

11.19 The Project Viva voce examinations shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who has adjudicated the dissertation. For Dissertation Evaluation (Viva voce) in IV Sem. there are external marks of 100 and it is evaluated by external examiner. The candidate has to secure a minimum of 50% marks in Viva voce exam.

11.20 If he fails to fulfill the requirements as specified, he will reappear for the Project Viva voce examination only after three months. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for the award of the degree.

12. Credits for Co-curricular Activities

The credits assigned for co-curricular activities shall be given by the principals of the colleges and the same shall be submitted to the University.

A Student shall earn 02 credits under the head of co-curricular activities, viz., attending Conference, Scientific Presentations and Other Scholarly Activities.

Following are the guidelines for awarding Credits for Co-curricular Activities

Name of the Activity	Maximum Credits / Activity
Participation in National Level Seminar/ Conference / Workshop /Training programs (related to the specialization of the student)	1
Participation in International Level Seminar / Conference / workshop/Training programs held outside India (related to the specialization of the student)	2
Academic Award/Research Award from State Level/National Agencies	1
Academic Award/Research Award from International Agencies	2
Research / Review Publication in National Journals (Indexed in Scopus / Web of Science)	1
Research / Review Publication in International Journals with Editorial board outside India (Indexed in Scopus / Web of Science)	2

Note:

i) Credit shall be awarded only for the first author. Certificate of attendance and participation in a Conference/Seminar is to be submitted for awarding credit.

ii) Certificate of attendance and participation in workshops and training programs (Internal or External) is to be submitted for awarding credit. The total duration should be at least one week.

iii) Participation in any activity shall be permitted only once for acquiring required credits under cocurricular activities

13. Grading:

As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades and corresponding percentage of marks shall be followed:

After each course is evaluated for 100 marks, the marks obtained in each course will be converted to a corresponding letter grade as given below, depending on the range in which the marks obtained by the student fall.

Structure of Grading of Academic Performance

Range in which the marks in the subject fall	Grade	Grade points Assigned
≥ 90	S (Superior)	10
≥ 80 < 90	A (Excellent)	9
≥ 70 < 80	B (Very Good)	8
≥ 60 < 70	C (Good)	7
≥ 50 < 60	D (Pass)	6
< 50	F (Fail)	0
Absent	Ab (Absent)	0

i) A student obtaining Grade 'F' or Grade 'Ab' in a subject shall be considered failed and will be required to reappear for that subject when it is offered the next supplementary examination.
ii) For noncredit audit courses, "Satisfactory" or "Unsatisfactory" shall be indicated instead of the letter grade and this will not be counted for the computation of SGPA/CGPA/Percentage.

Computation of Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):

The Semester Grade Point Average (SGPA) is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e.,

$$SGPA = \Sigma (C_i \times G_i)/\Sigma C_i$$

where, C_i is the number of credits of the i^{th} subject and G_i is the grade point scored by the student in the i^{th} course.

i) The Cumulative Grade Point Average (CGPA) will be computed in the same manner considering all the courses undergone by a student over all the semesters of a program, i.e.,

$$CGPA = \Sigma (C_i \times S_i)/ \Sigma C_i$$

where "S_i" is the SGPA of the i^{th} semester and C_i is the total number of credits up to that semester.
ii) Both SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.
iii) While computing the SGPA the subjects in which the student is awarded Zero grade points will also be included.

Grade Point: It is a numerical weight allotted to each letter grade on a 10-point scale.
Letter Grade: It is an index of the performance of students in a said course. Grades are denoted by letters S, A, B, C, D and F.

14. Award of Class:

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes:

Class Awarded	Percentage of Marks to be secured
First Class with Distinction	≥70%
First Class	< 70% ≥ 60%
Pass Class	< 60% ≥ 50%

15. **Exit Policy:** The student shall be permitted to exit with a PG Diploma based on his/her request to the university through the respective institution at the end of first year subject to passing all the courses in first year.

    The University shall resolve any issues that may arise in the implementation of this policy from time to time and shall review the policy in the light of periodic changes brought by UGC, AICTE and State government.

16. Withholding of Results:

If the candidate has any case of in-discipline pending against him, the result of the candidate shall be withheld, and he will not be allowed/promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

17. **Transitory Regulations**

Discontinued, detained, or failed candidates are eligible for readmission as and when the semester is offered after fulfilment of academic regulations. Candidates who have been detained for want of attendance or not fulfilled academic requirements or who have failed after having undergone the course in earlier regulations or have discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered, subject to Section 2 and they will follow the academic regulations into which they are readmitted.

18. General:

17.1 The academic regulations should be read as a whole for purpose of any interpretation.

17.2 Disciplinary action for Malpractice/improper conduct in examinations is appended.

17.3 There shall be no places transfer within the constituent colleges and affiliated colleges of Jawaharlal Nehru Technological University Anantapur.

17.4 Where the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

17.5 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chancellor is final.

17.6 The University may change or amend the academic regulations or syllabi at any time and the changes or amendments shall be made applicable to all the students on rolls with effect from the dates notified by the University.

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RULES FOR

DISCIPLINARY ACTION FOR MALPRACTICES / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	Punishment
	If the candidate:	
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University.
3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred for four consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for four consecutive semesters from class work and all University examinations if his involvement is established. Otherwise, the candidate is debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.

4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject only.
6.	Refuses to obey the orders of the Chief Superintendent /Assistant - Superintendent /any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. If the candidate physically assaults the invigilator/ officer-in-charge of the Examinations, then the candidate is also debarred and forfeits his/her seat. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project

		work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person (s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.
11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject only or in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester / year examinations, depending on the recommendation of the committee.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment.	

1. Malpractices identified by squad or special invigilators
2. Punishments to the candidates as per the above guidelines.
3. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)
4. A show cause notice shall be issued to the college.
5. Impose a suitable fine on the college.
6. Shifting the examination center from the college to another college for a specific period of not less than one year.

Note:

Whenever the performance of a student is cancelled in any subject/subjects due to Malpractice, he has to register for End Examinations in that subject/subjects consequently and has to fulfil all the norms required for the award of Degree.

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M.TECH. IN EMBEDDED SYSTEMS

COURSE STRUCTURE & SYLLABI

SEMESTER – I

S. No.	Course codes	Course Name	Category	Hours per			Credits
				L	T	P	
1.	21D06102	Microcontrollers and Programmable Digital Signal Processors	PC	3	0	0	3
2.	21D06101	Digital System Design with PLDs	PC	3	0	0	3
3.	21D55101a 21D57102 21D06103a	**Program Elective – 1** Advanced Microcontrollers CMOS Digital IC Design Advanced Computer Architectures	PE	3	0	0	3
4.	21D06203c 21D55102a 21D06203a	**Program Elective – 1** Embedded Real Time Operating Systems Advanced Computer Networks SoC Architecture	PE	3	0	0	3
5.	21D06105	Digital System Design Lab	PC	0	0	4	2
6.	21D06106	Microcontroller and Programmable Digital Signal Processors Lab	PC	0	0	4	2
7.	21DRM101	Research Methodology and IPR	MC	2	0	0	2
8.	21DAC101a 21DAC101b 21DAC101c	**Audit Course – I** English for Research paper writing Disaster Management Sanskrit for Technical Knowledge	AC	2	0	0	0
Total							**18**

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SEMESTER – II

S.No.	Course codes	Course Name	Category	Hours per week			Credits
				L	T	P	
1.	21D06201	Embedded System Design	PC	3	0	0	3
2.	21D55201	Embedded Programming	PC	3	0	0	3
3.	21D55202a 21D55202b	**Program Elective – III** Sensors and Actuators Modern Control Theory Artificial Intelligence and Machine Learning	PE	3	0	0	3
4.	21D06301b 21D06103b 21D06204a	**Program Elective – IV** Soft Computing Techniques Design of Fault Tolerant Systems Hardware and Software Co-design	PE	3	0	0	3
5.	21D06205	Embedded System Design Lab	PC	0	0	4	2
6.	21D55202	Embedded Programming Lab	PC	0	0	4	2
7.	21D55203	Technical seminar	PR	0	0	4	2
8.	21DAC201a 21DAC201b 21DAC201c	**Audit Course – II** Pedagogy Studies Stress Management for Yoga Personality Development through Life Enlightenment Skills	AC	2	0	0	0
Total							**18**

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SEMSTER - III

S.No.	Course codes	Course Name	Category	Hours per			Credits
					T	P	
1.	21D06301a 21D06301c 21D55301a	**Program Elective – V** Embedded Systems Protocols Communication Buses and Interfaces Robotics	PE	3	0	0	3
2.	21DOE301b 21DOE301c 21DOE301e	**Open Elective** Industrial Safety Business Analytics Waste to Energy	OE	3	0	0	3
3.	21D55302	Dissertation Phase – I	PR	0	0	20	10
4.	21D553013	Co-curricular Activities					2
		Total					**18**

SEMESTER - IV

S.No.	Course codes	Course Name	Category	Hours per week			Credits
				L	T	P	
1.	21D55401	Dissertation Phase – II	PR	0	0	32	16
Total							**16**

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

Course Code	MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS	L	T	P	C
21D06102		3	0	0	3
	Semester	I			

Course Objectives:

- To learn about ARM Microcontroller architectural features
- To understand the ARM 'C' Programming for various applications
- To study the DSP processor fundamentals and its development tools

Course Outcomes (CO): Student will be able to

- Learn about ARM Microcontroller architectural features
- Understand the ARM 'C' Programming for various applications
- Study the DSP processor fundamentals and its development tools

UNIT - I	Lecture Hrs:

ARM Cortex-Mx Processor: Applications, Programming model – Registers, Operation - modes, Exceptions and Interrupts, Reset Sequence, Instruction Set (ARM and Thumb), Unified AssemblerLanguage, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

UNIT - II	Lecture Hrs:

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

UNIT - III	Lecture Hrs:

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

UNIT - IV	Lecture Hrs:

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family

UNIT - V	Lecture Hrs:

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.

Textbooks:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition
2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications" , TMH, 2nd Edition.

Reference Books:

1. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication.
2. Steve furber, "ARM System-on-Chip Architecture", Pearson Education
3. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley
4. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com

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M.TECH. IN EMBEDDED SYSTEMS

COURSE STRUCTURE & SYLLABI

Course Code	DIGITAL SYSTEM DESIGN with PLDs	L	T	P	C
21D06101		3	0	0	3
Semester		I			

Course Objectives:

- To understand an overview of system design approach using programmable logic devices.
- To get exposed to the various architectural features of CPLDS and FPGAS.
- To learn the methods and techniques of CPLD & FPGA design with EDA tools.
- To learn software tools used for design process with the help of case studies.

Course Outcomes (CO): Student will be able to

- Understand an overview of system design approach using programmable logic devices.
- Get exposed to the various architectural features of CPLDS and FPGAS.
- Learn the methods and techniques of CPLD & FPGA design with EDA tools.
- Learn software tools used for design process with the help of case studies.

UNIT - I Lecture Hrs:

Programmable Logic Devices: The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, Xilinx CPLDs- Altera CPLDs, FPGAs-FPGA technology, architecture, CLB and slice Stratix LAB and ALM-RAM Blocks, Different types Xilinx FPGAs, DSP Blocks, Clock Management, I/O standards, Additional features.

UNIT - II Lecture Hrs:

Analysis and Derivation of Clocked Sequential Circuits with State Graphs and Tables: A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation

UNIT - III Lecture Hrs:

Sequential circuit Design: Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLDs, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design

UNIT - IV Lecture Hrs:

Fault Modeling and Test Pattern Generation: Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model.Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults.

UNIT - V Lecture Hrs:

Fault Diagnosis in Sequential Circuits: Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

Textbooks:

1.Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.
2. Fundamentals of Logic Design-Charles H.Roth,Jr. -5th Ed.,Cengage Learning.
3. Logic Design Theory-N.N.Biswas,PHI.

Reference Books:

1. Digital Circuits and Logic Design-Samuel C.LEE,PHI, 2008.
2. Digital System Design using programmable logic devices- Parag K.Lala, BS publications.

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

Course Code	ADVANCED MICROCONTROLLERS	L	T	P	C
21D55101a		3	0	0	3
	Semester	**I**			

Course Objectives:

- To explore the architecture and instruction set of ARM processor.
- To provide a comprehensive understanding of various programs of ARM Processors.
- To learn the programming on ARM Cortex M.

Course Outcomes (CO): Student will be able to

- Explore the selection criteria of ARM processors by understanding the functional level trade off issues.
- Explore the ARM development towards the functional capabilities.
- Expected to work with ASM level program using the instruction set.
- Understand the architecture of ARM Cortex M and programming on it.

UNIT - I Lecture Hrs:

ARM Embedded Systems
RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software.

ARM Processor Fundamentals
Registers, Current Program Status Register, Pipeline, Exceptions Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.

Architecture of ARM Processors
Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions?, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

UNIT - II Lecture Hrs:

Introduction to the Arm Instruction Set
Data processing instructions, branch instructions, load-store instructions, software interrupt instructions, program status register instructions, loading constants, ARMv5E extensions, Conditional execution.

Introduction to the Thumb Instruction Set
Thumb Register Usage, ARM-Thumb Interworking, Other Branch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple-Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

UNIT - III Lecture Hrs:

Technical Details of ARM Cortex M Processors
General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors-Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT - IV Lecture Hrs:

Instruction SET of ARM Cortex M
Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4-specific instructions,

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Barrel shifter, Accessing special instructions and special registers in Programming.		
UNIT - V		Lecture Hrs:
Floating Point Operations About Floating Point Data,Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1. ARM Cortex-M4 and DSP Applications: DSP on a microcontroller, Dot Product example, writing optimized DSP code for the CortexM4-Biquad filter, Fast Fourier transform, FIR filter.		
Textbooks:		
1. ARM System Developer's Guide Designing and Optimizing System Software by Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT, Elsevier Publications, 2004. 2. The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Joseph Yiu, Elsevier Publications, 3rdEdition.		
Reference Books:		
1. ARM System on Chip Architectures – Steve Furber, Edison Wesley, 2000. 2. ARM Architecture Reference Manual – David Seal, Edison Wesley, 2000.		

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

Course Code	CMOS DIGITAL IC DESIGN	L	T	P	C
21D57102		3	0	0	3
	Semester	I			

Course Objectives:

- To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
- The course also involves analysis of performance metrics.
- To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits.
- To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

Course Outcomes (CO): Student will be able to

- Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS,
- Estimate Delay and Power of Adders circuits.
- Classify different semiconductor memories.
- Analyze, design and implement combinational and sequential MOS logic circuits.
- Analyze complex engineering problems critically in the domain of digital IC design for conducting research.
- Solve engineering problems for feasible and optimal solutions in the core area of digital ICs

UNIT - I		Lecture Hrs:

MOS Design Pseudo NMOS Logic: Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT - II		Lecture Hrs:

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT - III		Lecture Hrs:

Sequential MOS Logic Circuits: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop

UNIT - IV		Lecture Hrs:

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT - V		Lecture Hrs:

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

Textbooks:

1. Neil Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Pearson, 2010
2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Edition, 2011.

Reference Books:

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1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M.Rabaey, AnanthaChandrakasan, Borivoje Nikolic, 2ndEdition, PHI.

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COURSE STRUCTURE & SYLLABI

Course Code	ADVANCED COMPUTER ARCHITECTURES	L	T	P	C
21D06103a		3	0	0	3
	Semester	**I**			

Course Objectives:

- To learn the instruction set architectures from a design perspective, including memory addressing, operands, and control flow.
- To understand the advanced concepts such as instruction level parallelism, , out-of-order execution, chip-multiprocessing and the related issues of data hazards, branch costs, hardware prediction.
- To study the multiprocessor and parallel processing architectures.
- To learn about the organization and design of contemporary processor architectures.

Course Outcomes (CO): Student will be able to

- Learn the instruction set architectures from a design perspective, including memory addressing, operands, and control flow.
- Understand the advanced concepts such as instruction level parallelism, out-of-order execution, chip-multiprocessing and the related issues of data hazards, branch costs, hardware prediction.
- Study the multiprocessor and parallel processing architectures.
- Learn about the organization and design of contemporary processor architectures.

UNIT - I		Lecture Hrs:

Fundamentals of Computer Design
Fundamentals of Computer design, Changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law.
Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT - II		Lecture Hrs:

Pipelines
Introduction ,basic RISC instruction set ,Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining , Pipeline hazards, Reducing pipeline branch penalties.
Memory Hierarchy Design
Introduction, review of fundamentals of cache, Cache performance , Reducing cache miss penalty, Virtual memory.

UNIT - III		Lecture Hrs:

Instruction Level Parallelism the Hardware Approach
Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.
ILP Software Approach
Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT - IV		Lecture Hrs:

Multi Processors and Thread Level Parallelism
Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT - V		Lecture Hrs:

Inter Connection and Networks

Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters. **Intel Architecture** Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls.
Textbooks:
1. John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier.
Reference Books:
1. John P. Shen and Miikko H. Lipasti, Modern Processor Design : Fundamentals of Super Scalar Processors 2. Computer Architecture and Parallel Processing ,Kai Hwang, Faye A.Brigs., MC Graw Hill., 3. Advanced Computer Architecture - A Design Space Approach, DezsoSima, Terence Fountain, Peter Kacsuk ,Pearson Ed.,

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

Course Code	EMBEDDED REAL TIME OPERATING SYSTEMS	L	T	P	C
21D06203c		3	0	0	3
	Semester	**I**			

Course Objectives:

- To provide broad understanding of the requirements of Real Time Operating Systems.
- To make the student understand, applications of these Real Time features using case studies.
- To use the real time operating system concepts.

Course Outcomes (CO): Student will be able to

- Acquire knowledge on Real Time features of UNIX and LINUX.
- Understand the basic building blocks of Real Time Operating Systems in terms of scheduling, context switching and ISR.
- Understand on Real Time applications using Real Time Linux, ucos2, VX works, Embedded Linux.

UNIT - I	Lecture Hrs:

Introduction
Introduction to UNIX/LINUX, Overview of Commands, File I/O,(open, create, close, lseek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT - II	Lecture Hrs:

Real Time Operating Systems
Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.
Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use.

UNIT - III	Lecture Hrs:

Objects, Services and I/O
Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem.

UNIT - IV	Lecture Hrs:

Exceptions, Interrupts and Timers
Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT - V	Lecture Hrs:

Case Studies of RTOS
RT Linux, MicroC/OS-II, Vx Works, Embedded Linux, and Tiny OS.

Textbooks:

1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011.

Reference Books:

1. Embedded Systems- Architecture, Programming and Design by Rajkamal,TMH, 2007.
2. Advanced UNIX Programming, Richard Stevens.
3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh.

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COURSE STRUCTURE & SYLLABI

Course Code	ADVANCED COMPUTER NETWORKS	L	T	P	C
21D55102a		3	0	0	3
	Semester	I			

Course Objectives:

- To understand various protocols in computer networks
- To learn about congestion control and quality of service in computer networks
- To study various aspects of adhoc wireless networks
- To study various aspects of wireless sensor networks

Course Outcomes (CO): Student will be able to

- Understand various protocols in computer networks
- Learn about congestion control and quality of service in computer networks
- Study various aspects of adhoc wireless networks
- Study various aspects of wireless sensor networks

UNIT - I		Lecture Hrs:

Wireless LANs
Architectural Comparison, Characteristics, Access Control, IEEE 802.11 Project: Architecture, MAC Sub layer, Addressing Mechanism, Physical Layer, Bluetooth Architecture, Bluetooth Layers, ZigBee, WiMAX Services, IEEE Project 802.16, Cellular Telephony: operation,1G,2G,3G,4G,5G Satellite Networks, GEO, MEO and LEO Satellites

UNIT - II		Lecture Hrs:

Congestion Control and Quality of Service
Data Traffic, Congestion, Congestion Control, Quality of Service, Techniques to Improve QoS, Integrated Services, Differentiated Services, QoS in Switched Networks,Queue Management ,Passive-Drop trial, Drop front, Random drop, Active- early Random drop, Random Early detection.

UNIT - III		Lecture Hrs:

AD HOC WIRELESS NETWORKS
Introduction, Cellular and Ad hoc Wireless Networks, Application of Ad Hoc Wireless Networks, Issues in Ad Hoc Wireless Networks, Medium Access Scheme, Routing, Multicasting, Transport Layer Protocols, Pricing Scheme, Quality of Service Provisioning, Self-Organization, Security, Addressing and Service Discovery, Energy Management, Scalability, Deployment Considerations, Ad Hoc Wireless Internet

UNIT - IV		Lecture Hrs:

Quality of Service in Ad Hoc Wireless Networks
Introduction, Real Time Traffic Support in Ad Hoc Wireless Networks, QoS Parameters in Ad Hoc Wireless Network, Issues and Challenges in providing QoS in Ad Hoc Wireless Networks, Classification of QoS Solutions: MAC Layer Solutions, Cluster TDMA, IEEE 802.11e, DBASE, Network Layer Solutions, QoS Routing Protocols, Ticket Based QoS Routing Protocol, Predictive Location Based QoS routing protocol, Trigger Based Distributed QoS Routing Protocol, QoS enabled AODV Routing Protocol, Bandwidth QoS Routing Protocol, On Demand QoS Routing Protocol, On Demand Link-State Multipath QoS Routing Protocol, Asynchronous Slot Allocation Strategies. QoS Frameworks for Ad Hoc Wireless Networks.

UNIT - V		Lecture Hrs:

Wireless Sensor Networks
Introduction, Application of Sensor Network , Comparison with Ad hoc Wireless Networks, Issues and challenges in Designing a Sensor Network, Sensor Network Architecture, Layer Architecture,

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Cluster Architecture, Data Dissemination Flooding, Gossiping, Rumor Routing, Sequential Assignment Routing, Direct Diffusion, Sensor Protocols for Information via Negotiation, Cost- Field Approach, Geography Hash Table, Small Minimum Energy Communication Network, Data Gathering, Direct Transmission, Power Efficient Gathering for Sensor Information Systems, Binary Scheme, Chain Based Three-Level Scheme.
Textbooks:
1.Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI 2.Data Communications and Networking - B. A.Forouzan, 5th , 2013, TMH.
Reference Books:
1.Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI. 2.Data and Computer Communications - William Stallings, 8th ed., 2007, PHI.

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M.TECH. IN EMBEDDED SYSTEMS

COURSE STRUCTURE & SYLLABI

Course Code	SoC ARCHITECTURE	L	T	P	C
21D06203a		3	0	0	3
	Semester	I			

Course Objectives:

- To understand the basics related to SoC architecture and different approaches related to SoC Design.
- To select an appropriate robust processor for SoC Design
- To select an appropriate memory for SoC Design.
- To realize real time case studies

Course Outcomes (CO): Student will be able to

- Understand the basics related to SoC architecture and different approaches related to SoC Design.
- Select an appropriated robust processor for SoC Design
- Select an appropriate memory for SoC Design.
- Realize real time case studies

UNIT - I Lecture Hrs:

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory &Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT - II Lecture Hrs:

Processors: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Microarchitecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instruction extensions, VLIW Processors, Superscalar Processors

UNIT - III Lecture Hrs:

Memory Design for SOC: Overview: SOC external memory, SOC Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Other Types of Cache, Split – I, and D – Caches, Multilevel Caches, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT - IV Lecture Hrs:

Interconnect, Customization and Configurability: Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

SOC Customization: An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT - V Lecture Hrs:

Application Studies / Case Studies: SOC Design approach; AES-algorithms, Design and evaluation; Image compression–JPEG compression.

Textbooks:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber, 2ndEdition, 2000, Addison Wesley Professional.

Reference Books:

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2.Co-Verification of Hardware and Software for ARM System on Chip Design (EmbeddedTechnology) – Jason Andrews – Newnes, BK and CDROM.
3.System on Chip Verification – Methodologies and Techniques –PrakashRashinkar, PeterPaterson and Leena Singh L, 2001, Kluwer Academic Publishers

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M.TECH. IN EMBEDDED SYSTEMS

COURSE STRUCTURE & SYLLABI

Course Code	DIGITAL SYSTEM DESIGN LAB	L	T	P	C
21D06105		0	0	4	2
	Semester	I			

Course Objectives:

- To familiarize the HDL simulator / synthesis tool
- To design and implement given combinational circuit on FPGA device
- To design and implement given sequential circuit on FPGA device

Course Outcomes (CO):

- Familiarize the HDL simulator / synthesis tool
- Design and implement given combinational circuit on FPGA device
- Design and implement given sequential circuit on FPGA device

List of Experiments:

Student has to design his/her user defined library components by using and standard HDL simulator / Synthesis tool for target FPGA device.

1. Combinational Logic Circuits
    a. Generic Multiplexer.
    b. Generic Priority Encoder.
    c. Design of RAM Memory.
    d. Code Converters.
    e. Combinational Arithmetic circuits
    f. Ripple Carry Adder.
    g. Carry-Look ahead adder.
    h. Signed and Unsigned Adders.
    i. Signed and Unsigned Subtractors.
    j. N-bit Comparator.
    k. N – bit Arithmetic Logic Unit.
    l. Parallel Signed and unsigned Multipliers.
    m. Dividers.
2. Sequential Circuits
    a. Shift Register with Load.
    b. Switch Debouncer.
    c. Timer.
    d. Fibonacci Series Generator.
    e. Frequency Meters.

Software Requirements:
Xilinx Vivado, Intel Quartus Prime Pro, Lattice Diamond, equivalent EDA software
Hardware Requirements:
Xilinx / Altera / Lattice / Equivalent FPGA development kits

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

Course Code	MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS LAB	L	T	P	C
21D06106		0	0	4	2
	Semester	I			

Course Objectives:

- To write the ARM 'C' programming for applications
- To understand the interfacing of various modules with ARM 7/ ARM Cortex-M3
- To develop assembly and C Programming for DSP processors

Course Outcomes (CO):

- Install, configure and utilize tool sets for developing applications based on ARM processor core.
- Design and developtheARM7 based embedded systems for various applications.
- Develop application programs on ARM and DSP development boards both in assembly and C.
- Design and Implement the digital filters on DSP6713 processor.
- Analyze the hardware and software interaction and integration.

List of Experiments:

Part A) Experiments to be carried out on Cortex-Mx development boards and using GNU tool-chain

1. Blink an LED with software delay, delay generated using the SysTick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

Part B) Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

12. To develop an assembly code and C code to compute Euclidian distance between any two points
13. To develop assembly code and study the impact of parallel, serial and mixed execution
14. To develop assembly and C code for implementation of convolution operation
15. To design and implement filters in C to enhance the features of given input sequence/signa

Software Requirements:
Keil for ARM, Code Composer Studio
Hardware Requirements:
ARM Cortex Mx Development Boards, TI TMS C6713 evaluation kit

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M.TECH. IN EMBEDDED SYSTEMS

COURSE STRUCTURE & SYLLABI

Course Code	**RESEARCH METHODOLOGY AND IPR**	**L**	**T**	**P**	**C**
21DRM101		**2**	**0**	**0**	**2**
	Semester		**I**		

Course Objectives:

- Identify an appropriate research problem in their interesting domain.
- Understand ethical issues understand the Preparation of a research project thesis report.
- Understand the Preparation of a research project thesis report
- Understand the law of patent and copyrights.
- Understand the Adequate knowledge on IPR

Course Outcomes (CO): Student will be able to

- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT - I		Lecture Hrs:

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, scope, and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT - II		Lecture Hrs:

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT - III		Lecture Hrs:

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT - IV		Lecture Hrs:

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT - V		

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Textbooks:

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

Reference Books:

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step by Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.

5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, " Intellectual Property in New
7. Technological Age", 2016.

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M.TECH. IN EMBEDDED SYSTEMS

COURSE STRUCTURE & SYLLABI

Course Code	EMBEDDED SYSTEMS DESIGN	L	T	P	C
21D06201		3	0	0	3
	Semester	II			

Course Objectives:

- To differentiate between a General purpose and an Embedded System.
- To provide knowledge on the building blocks of Embedded System.
- To understand the requirement of Embedded firmware and its role in API.

Course Outcomes (CO): Student will be able to

- Expected to differentiate the design requirements between General Purpose and Embedded Systems.
- Expected to acquire the knowledge of firmware design principles.
- Expected to understand the role of Real Time Operating System in Embedded Design.
- To acquire the knowledge and experience of task level Communication in any Embedded System.

UNIT - I — Lecture Hrs:

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems,
Characteristics and Quality Attributes of Embedded Systems.

UNIT - II — Lecture Hrs:

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces. DDR , Flash, NVRAM

UNIT - III — Lecture Hrs:

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT - IV — Lecture Hrs:

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT - V — Lecture Hrs:

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

Textbooks:

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

Reference Books:

1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

Course Code	EMBEDDED PROGRAMMING	L	T	P	C
21D55201		3	0	0	3
	Semester	**II**			

Course Objectives:

- To explore the difference between general purpose programming languages and Embedded Programming Language.
- To provide case studies for programming in Embedded systems.

Course Outcomes (CO): Student will be able to

- Learn the basics of Embedded C with reference to 8051.
- Understand how to handle control and data pins at hardware level.
- Introduce objective nature of Embedded C.
- Understand the specifications of real time embedded programming with case studies.

UNIT - I — Lecture Hrs:

PROGRAMMING EMBEDDED SYSTEMS IN C: Introduction to embedded system, Processor used, programming language used, operating system used, developing embedded software.
INTRODUCING THE 8051 MICROCONTROLLER FAMILY: Introduction, The external interface of the Standard 8051, Reset requirements, Clock frequency and performance Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption.

UNIT - II — Lecture Hrs:

EMBEDDED WORLD: Introduction Installing the Keil software and loading the project, Configuring the simulator, Building the target, Running the simulation, Dissecting the program, Building the hardware.

UNIT - III — Lecture Hrs:

READING SWITCHES: Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version),The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code).

UNIT - IV — Lecture Hrs:

ADDING STRUCTURE TO YOUR CODE: Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example.
MEETING REAL-TIME CONSTRAINTS: Introduction, Creating 'hardware delays' using Timer 0 and Timer, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, The need for 'timeout' mechanisms, Creating loop timeouts.

UNIT - V — Lecture Hrs:

CREATING AN EMBEDDED OPERATING SYSTEM: Introduction, The basis of a simple embedded OS, Introducing sEOS, Using Timer 0 or Timer 1, alternative architectures, important design considerations when using sEOS.
MULTI-STATE SYSTEMS AND FUNCTION SEQUENCES: Introduction, Implementing a Multi-State (Timed) system, traffic light sequencing, Animatronics dinosaur, implementing a Multi-State (Input/Timed) system, Controller for a washing machine

Textbooks:

1. Embedded C By Micheal J. Pont Pearson Education, 2002.
2. Embedded C Coding standard-Michael Barr from Neutrino.

Reference Books:

1. Real Time Concepts for Embedded systems-Qing Li,Caroline Yao, CMP Books 2003.
2. Embedded/Real Time Syatems-KVKK Prasad, Dreamtech press,2005

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

Course Code	SENSORS AND ACTUATORS	L	T	P	C
21D55202a		3	0	0	3
	Semester	**II**			

Course Objectives:

- To Learn about Electro mechanical sensors.
- To Learn the use of the thermal sensors and magnetic sensors for embedded system.
- To learn the basics of radiation sensors, smart sensors and actuators.

Course Outcomes (CO): Student will be able to

- Learn about Electro mechanical sensors.
- Learn the use of the thermal sensors and magnetic sensors for embedded system.
- Learn the basics of radiation sensors, smart sensors and actuators.

UNIT - I Lecture Hrs:

Sensors/Transducers
Principles – Classification – Parameters – Characteristics - Environmental Parameters (EP) – Characterization.
Mechanical and Electromechanical Sensors
Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor –Types-Capacitive Sensors:– Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors.

UNIT - II Lecture Hrs:

Thermal Sensors
Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermosensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors –Thermoemf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors – NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry – Heat Flux Sensors.
Magnetic sensors
Introduction – Sensors and the Principles Behind – Magneto-resistive Sensors – Anisotropic Magnetoresistive Sensing – Semiconductor Magnetoresistors– Hall Effect and Sensors – Inductance and Eddy Current Sensors– Angular/Rotary Movement Transducers – Synchros – Synchro-resolvers - Eddy Current Sensors – Electromagnetic Flowmeter – Switching Magnetic Sensors SQUID Sensors.

UNIT - III Lecture Hrs:

Radiation Sensors
Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors.
Electro analytical Sensors
Introduction – The Electrochemical Cell – The Cell Potential - Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization-– Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media.

UNIT - IV Lecture Hrs:

Smart Sensors
Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The Automation.

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M.TECH. IN EMBEDDED SYSTEMS

COURSE STRUCTURE & SYLLABI

Sensors –Applications Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors — Sensors for Manufacturing –Sensors for environmental Monitoring.		
UNIT - V		Lecture Hrs:
Actuators Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Presure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators. Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection. Electrical Actuation Systems-Electrical systems -Mechanical switches – Solid-state switches Solenoids – D.C. Motors – A.C. motors – Stepper motors.		
Textbooks:		
1.D. Patranabis, “Sensors and Transducers”, PHI Learning Private Limited. 2. W. Bolton, “Mechatronics”, Pearson Education Limited.		
Reference Books:		
1. Ernest O.Doebelin, Measurement Systems - Application & Design,4th Edition,Mc-GrawHill Publishing company 2. C. Rangan , G Sarma , V.S.V. Mani Instrumentation: Devices and Systems,4th Edition,Mc-GrawHill Publishing company		

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

Course Code	MODERN CONTROL THEORY	L	T	P	C
21D55202b		3	0	0	3
	Semester	**II**			

Course Objectives:

- To understand concepts of modern control system To explain the concepts of state variables analysis.
- To study and analyze non linear control systems.
- To analyze the concept of stability for nonlinear control systems and their categorization.
- To apply the comprehensive knowledge of optimal theory for Control Systems.

Course Outcomes (CO): Student will be able to

- Understand concepts of modern control system To explain the concepts of state variables analysis.
- Study and analyze non linear control systems.
- Analyze the concept of stability for nonlinear control systems and their categorization.
- Apply the comprehensive knowledge of optimal theory for Control Systems.

UNIT - I Lecture Hrs:

Mathematical Preliminaries and State Variable Analysis
Fields, Vectors and Vector Spaces – Linear combinations and Bases – Linear Transformations and Matrices – Scalar Product and Norms – Eigen values, Eigen Vectors and a Canonical form representation of Linear systems – The concept of state – State space model of Dynamic systems – Time invariance and Linearity – Non uniqueness of state model – State diagrams for Continuous-Time State models - Existence and Uniqueness of Solutions to Continuous-Time State Equations – Solutions of Linear Time Invariant Continuous-Time State Equations – State transition matrix and it's properties. Complete solution of state space model due to zero input and due to zero state.

UNIT - II Lecture Hrs:

Controllability and Observability
General concept of controllability – Controllability tests, different state transformations such as diagonalization, Jordon canonical forms and Controllability canonical forms for Continuous-Time Invariant Systems – General concept of Observability – Observability tests for Continuous-Time Invariant Systems – Observability of different State transformation forms.

UNIT - III Lecture Hrs:

State Feedback Controllers and Observers
State feedback controller design through Pole Assignment, using Ackkermans formula– State observers: Full order and Reduced order observers.

UNIT - IV Lecture Hrs:

Non-Linear Systems
Introduction – Non Linear Systems - Types of Non-Linearities – Saturation – Dead-Zone - Backlash – Jump Phenomenon etc; Linearization of nonlinear systems, Singular Points and its types– Describing function–describing function of different types of nonlinear elements, – Stability analysis of Non-Linear systems through describing functions. Introduction to phase-plane analysis, Method of Isoclines for Constructing Trajectories, Stability analysis of nonlinear systems based on phase-plane method.

UNIT - V Lecture Hrs:

Stability Analysis
Stability in the sense of Lyapunov, Lyapunov's stability and Lypanov's instability theorems - Stability Analysis of the Linear continuous time invariant systems by Lyapunov second method – Generation of Lyapunov functions – Variable gradient method – Krasooviski's method.

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COURSE STRUCTURE & SYLLABI

Textbooks:
1. M.Gopal, Modern Control System Theory, New Age International - 1984 2. Ogata. K, Modern Control Engineering, Prentice Hall - 1997 3. N K Sinha, Control Systems, New Age International – 3rd edition.
Reference Books:
1. Donald E.Kirk, Optimal Control Theory an Introduction, Prentice - Hall Network series - First edition.

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

Course Code	ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING	L	T	P	C
21D38301b		3	0	0	3
Semester		II			

Course Objectives:

- To learn the difference between optimal reasoning vs human like reasoning
- To understand the notions of state space representation, exhaustive search, heuristic search along with the time and space complexities
- To learn different knowledge representation techniques
- To understand the applications of Al: namely Game Playing, Theorem Proving, Expert Systems, Machine Learning and Natural. Language Processing

Course Outcomes (CO): Student will be able to

- Possess the ability to formulate an efficient problem space for a problem expressed in English.
- Possess the ability to select a search algorithm for a problem and characterize its time and space complexities.
- Possess the skill for representing knowledge using the appropriate technique.
- Possess the ability to apply Al techniques to solve problems of Game Playing, Expert Systems, Machine Learning and Natural Language Processing.

UNIT - I — Lecture Hrs:

Introduction, History, Intelligent Systems, Foundations of AI, Sub areas of AI, Applications. Problem Solving – State-Space Search and Control Strategies: Introduction, General Problem Solving, Characteristics of Problem, Exhaustive Searches, Heuristic Search Techniques, Iterative-Deepening A*, Constraint Satisfaction. Game Playing, Bounded Look-ahead Strategy and use of Evaluation Functions, Alpha-Beta Pruning

UNIT - II — Lecture Hrs:

Logic Concepts and Logic Programming
Introduction, Propositional Calculus, Propositional Logic, Natural Deduction System, Axiomatic System, Semantic Tableau System in Propositional Logic, Resolution Refutation in Propositional Logic, Predicate Logic, Logic Programming. Knowledge Representation: Introduction, Approaches to Knowledge Representation, Knowledge Representation using Semantic Network, Extended Semantic Networks for KR, Knowledge Representation using Frames.

UNIT - III — Lecture Hrs:

Expert System and Applications
Introduction, Phases in Building Expert Systems, Expert System Architecture, Expert Systems Vs Traditional Systems, Truth Maintenance Systems, Application of Expert Systems, List of Shells and Tools. Uncertainty Measure – Probability Theory: Introduction, Probability Theory, Bayesian Belief Networks, Certainty Factor Theory, Dempster-Shafer Theory.

UNIT - IV — Lecture Hrs:

Machine-Learning Paradigms
Introduction. Machine Learning Systems.Supervised and Unsupervised Learning. Inductive Learning. Learning Decision Trees (Text Book 2), Deductive Learning. Clustering, Support Vector Machines. Artificial Neural Networks: Introduction, Artificial Neural Networks, Single- Layer Feed-Forward Networks, Multi-Layer Feed-Forward Networks, Radial- Basis Function Networks, Design Issues of Artificial Neural Networks, Recurrent Networks.

UNIT - V — Lecture Hrs:

Advanced Knowledge Representation Techniques
Case Grammars, Semantic Web Natural Language Processing: Introduction, Sentence Analysis

Phases, Grammars and Parsers, Types of Parsers, Semantic Analysis, Universal Networking Knowledge.
Textbooks:
1. Saroj Kaushik. Artificial Intelligence. Cengage Learning, 2011. 2. Russell, Norvig: Artificial intelligence, A Modern Approach, Pearson Education, Second Edition. 2004.
Reference Books:
1. Rich, Knight, Nair: Artificial intelligence, Tata McGraw Hill, Third Edition 2009.

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

Course Code	SOFT COMPUTING TECHNIQUES	L	T	P	C
21D06301b		3	0	0	3
	Semester	**II**			

Course Objectives:

- To understand the concepts of different types neural networks
- To understand the concepts of fuzzy logic systems
- To learn concepts of genetic algorithm

Course Outcomes (CO): Student will be able to

- Understand the concepts of different types neural networks
- Understand the concepts of fuzzy logic systems
- Learn concepts of genetic algorithm

UNIT - I Lecture Hrs:

Fundamentals of Neural Networks & Feed Forward Networks: Basic Concept of Neural Networks, Human Brain, Models of an Artificial Neuron, Learning Methods, Neural Networks Architectures.
Feed Forward Neural Network: Single Layer Feed Forward Neural Network, The Perceptron Model,
Multilayer Feed Forward Neural Network, Architecture of a Back Propagation Network(BPN), The Solution, Backpropagation Learning, Selection of various Parameters in BPN. Application of Back propagation Networks in Pattern Recognition & Image Processing.

UNIT - II Lecture Hrs:

Associative Memories & ART Neural Networks: Basic concepts of Linear Associator, Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks(HPF), Mathematical Foundation of Gradient-Type Hopfield Networks, Transient response of Continuous Time Networks, Applications of HPF in Solution of Optimization Problem: Minimization of the Traveling salesman tour length, Summing networks with digital outputs, Solving Simultaneous Linear Equations, Bidirectional Associative Memory Networks; Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture

UNIT - III Lecture Hrs:

Fuzzy Logic & Systems: Fuzzy sets, Crisp Relations, Fuzzy Relations, Crisp Logic, Predicate Logic, Fuzzy Logic, Fuzzy Rule based system, Defuzzification Methods, Applications: Greg Viot's Fuzzy Cruise Controller, Air Conditioner Controller.

UNIT - IV Lecture Hrs:

Genetic Algorithms: Basic Concepts of Genetic Algorithms (GA), Biological background, Creation of Offsprings, Working Principle, Encoding, Fitness Function, Reproduction, Inheritance Operators, Cross Over, Inversion and Deletion, Mutation Operator, Bit-wise Operators used in GA, Generational Cycle, Convergence of Genetic Algorithm.

UNIT - V Lecture Hrs:

Hybrid Systems: Types of Hybrid Systems, Neural Networks, Fuzzy Logic, and Genetic Algorithms Hybrid, Genetic Algorithm based BPN: GA Based weight Determination, Fuzzy Back Propagation Networks: LR-type fuzzy numbers, Fuzzy Neuron, Fuzzy BP Architecture, Learning in Fuzzy BPN, Inference by fuzzy BPN.

Textbooks:

1.Introduction to Artificial Neural Systems - J.M.Zurada, Jaico Publishers
2.Neural Networks, Fuzzy Logic & Genetic Algorithms: Synthesis & Applications -S.Rajasekaran, G.A. VijayalakshmiPai, July 2011, PHI, New Delhi.
3.Genetic Algorithms by David E. Gold Berg, Pearson Education India, 2006.

4.Neural Networks & Fuzzy Sytems- Kosko.B., PHI, Delhi,1994.
Reference Books:
1.Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi. 2.An introduction to Genetic Algorithms - Mitchell Melanie, MIT Press, 1998 3.Fuzzy Sets, Uncertainty and Information- Klir G.J. & Folger. T. A., PHI, Delhi, 1993.

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

Course Code	DESIGN OF FAULT TOLERANT SYSTEMS	L	T	P	C
21D06103b		3	0	0	3
Semester		II			

Course Objectives:

- To provide broad understanding of fault diagnosis and tolerant design approach.
- To illustrate the framework of test pattern generation using semi and full automatic approach.
- To acquire the knowledge of scan architectures.
- To acquire the knowledge of design of built-in-self test.

Course Outcomes (CO): Student will be able to

- Provide broad understanding of fault diagnosis and tolerant design approach.
- Illustrate the framework of test pattern generation using semi and full automatic approach.
- Acquire the knowledge of scan architectures.
- Acquire the knowledge of design of built-in-self test.

UNIT - I Lecture Hrs:

Fault Tolerant Design
Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits.
Fault Tolerant Design
Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts.

UNIT - II Lecture Hrs:

Self Checking circuits & Fail safe Design
Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.
Fail Safe Design- Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design

UNIT - III Lecture Hrs:

Design for Testability
Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller's expansion technique, use of control and syndrome testable designs.
Design for testability by means of scan
Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip-flop Structures, Full scan design and Test, Scan Architectures-full scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.

UNIT - IV Lecture Hrs:

Logic Built-in-self-test
BIST Basics-Memory-based BIST,BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback shift register, Output Response Analysis-Engaging ORA's, One's counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralised and separate Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket(RTS), LSSD On-chip self test, Self –testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing coverage, RT level BIST design-CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results.

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COURSE STRUCTURE & SYLLABI

UNIT - V		Lecture Hrs:
Standard IEEE Test Access Methods Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language.		
Textbooks:		
1. Fault Tolerant & Fault Testable Hardware Design- Parag K.Lala,PHI, 1984. 2. Digital System Test and Testable Design using HDL models and Architectures - ZainalabedinNavabi, Springer International Ed.,		
Reference Books:		
1. Digital Systems Testing and Testable Design-MironAbramovici, Melvin A.Breuer and Arthur D. Friedman, Jaico Books 2. Essentials of Electronic Testing- Bushnell &VishwaniD.Agarwal,Springers. 3. Design for Test for Digital IC's and Embedded Core Systems- Alfred L. Crouch, 2008		

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

Course Code	HARDWARE AND SOFTWARE CO-DESIGN	L	T	P	C
21D06204a		3	0	0	3
	Semester	II			

Course Objectives:

- To acquire the knowledge on various models of Co-design.
- To explore the interrelationship between Hardware and software in a embedded system
- To acquire the knowledge of firmware development process and tools during Co-design.
- To understand validation methods and adaptability.

Course Outcomes (CO): Student will be able to

- Acquire the knowledge on various models of Co-design.
- Explore the interrelationship between Hardware and software in a embedded system
- Acquire the knowledge of firmware development process and tools during Co-design.
- Understand validation methods and adaptability.

UNIT - I	Lecture Hrs:

Co- Design Issues
Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. Co- Synthesis Algorithms
Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT - II	Lecture Hrs:

Prototyping and Emulation
Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.
Target Architectures
Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT - III	Lecture Hrs:

Compilation Techniques and Tools for Embedded Processor Architectures
Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT - IV	Lecture Hrs:

Design Specification and Verification
Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT - V	Lecture Hrs:

Languages for System – Level Specification and Design-I
System – level specification, design representation for system level synthesis, system level specification languages,
Languages for System – Level Specification and Design-II
Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Textbooks:

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1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – Springer, 2009.
2. Hardware / Software Co- Design - Giovanni De Micheli, MariagiovannaSami,Kluwer Academic Publishers, 2002.

Reference Books:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont, Springer, 2010.

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

Course Code	EMBEDDED SYSTEM DESIGN LAB	L	T	P	C
21D06205		0	0	4	2
	Semester	**II**			

Course Objectives:

- To familiarize with embedded systems programming concepts
- To implement different embedded communication and interfacing protocols

Course Outcomes (CO):

- Familiarize with embedded systems programming concepts
- Implement different embedded communication and interfacing protocols

List of Experiments:

1. Functional Testing of Devices
Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.
2. Exporting Display on to other Systems
Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
3. GPIO Programming
Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
4. Interfacing Chronos eZ430
Chronos device is a programmable Texas Instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.
5. ON/OFF Control Based On Light Intensity
Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value.
6. Battery Voltage Range Indicator
Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 LEDs, turn on 3 LED s for 2-3V, 2 LEDs for 1-2V, 1 LED for 0.1-1V & turn off all for 0V)
7. Dice Game Simulation
Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.
8. Displaying RSS News Feed On Display Interface
Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.
9. Porting Open w.r.t the Device
Attempt to use the device while connecting to a WiFi network using a USB dongle and at the same time providing a wireless access point to the dongle.
10. Hosting a website on Board
Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server (eg: Apache) and thereby host the website.
11. Webcam Server

Interfacing the regular USB webcam with the device and turn it into fully functional IP webcam & test the functionality.

12. FM Transmission

Transforming the device into a regular FM transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

Software Requirements:
Keil / Python
Hardware Requirements:
Arduino/Raspbery Pi/Beaglebone

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

Course Code	EMBEDDED PROGRAMMING LAB	L	T	P	C
21D55202		0	0	4	2
	Semester	II			

Course Objectives:

- To understand the concepts of Embedded 'C' programming
- To implement given program on 8051 microcontroller
- To implement given program on LPC2148 microcontroller

Course Outcomes (CO):

- Understand the concepts of Embedded 'C' programming
- Implement given program on 8051 microcontroller
- Implement given program on LPC2148 microcontroller

List of Experiments:

Embedded C programming and testing using 8051 advanced development board and KEIL tools.

1. (i) Program to perform arithmetic operations.
   (ii) Program to perform sorting of numbers.
2. Program to shift LED's Left and right.
3. Program for DIP switch interface.
4. Program to display message in LCD 8 bit mode.
5. Program to display picture in GLCD 128X64.
6. Program to send data serially through serial port.
7. Program to display I2C RTC(DS1307) to Hyper terminal window.
8. Program to display digital temperature sensor output.
9. Program for 4X4 matrix keyboard with LCD.
10. Program to interface stepper motor.
11. Program to interface relay.

Embedded C programming and testing using LPC2148 development kit(Real time environment)

1. Program to interface LED and implement Multi-tasking.
2. Program to display RTC-ADC on LCD.
3. Program to display message on GLCD

Software Requirements:
Keil for C51, Keil for ARM
Hardware Requirements:
8051 Development boards, LPC2148 Development boards

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M.TECH. IN EMBEDDED SYSTEMS

COURSE STRUCTURE & SYLLABI

Course Code	EMBEDDED SYSTEMS PROTOCOLS	L	T	P	C
21D06301a		3	0	0	3
	Semester	III			

Course Objectives:

- To acquire knowledge on communication protocols of connecting Embedded Systems.
- To understand the design parameters of USB and CAN bus protocols.
- To understand the design issues of Ethernet in Embedded networks.
- To acquire the knowledge of wireless protocols in Embedded domain.

Course Outcomes (CO): Student will be able to

- Acquire knowledge on communication protocols of connecting Embedded Systems.
- Understand the design parameters of USB and CAN bus protocols.
- Understand the design issues of Ethernet in Embedded networks.
- Acquire the knowledge of wireless protocols in Embedded domain.

UNIT - I — Lecture Hrs:

Embedded Communication Protocols
Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols – Firewire.

UNIT - II — Lecture Hrs:

USB and CAN Bus
USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN.

UNIT - III — Lecture Hrs:

Ethernet Basics
Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol.

UNIT - IV — Lecture Hrs:

Embedded Ethernet
Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT - V — Lecture Hrs:

Wireless Embedded Networking
Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing.

Textbooks:

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002.
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

Reference Books:

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COURSE STRUCTURE & SYLLABI

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors - BhaskarKrishnamachari□, Cambridge press 2005.

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M.TECH. IN EMBEDDED SYSTEMS

COURSE STRUCTURE & SYLLABI

Course Code	COMMUNICATION BUSES AND INTERFACES	L	T	P	C
21D06301c		3	0	0	3
	Semester	III			

Course Objectives:

- To understand the concepts of different types of serial buses.
- To learn about CAN, PCIe and USB architecture
- To learn about data streaming using serial communication protocols

Course Outcomes (CO): Student will be able to

- Understand the concepts of different types of serial buses.
- Learn about CAN, PCIe and USB architecture
- Learn about data streaming using serial communication protocols

UNIT - I Lecture Hrs:

Serial Busses- Cables, Serial busses, serial versus parallel, Data and Control Signal- data frame, data rate, features, Limitations and applications of RS232, RS485, I2C , SPI

UNIT - II Lecture Hrs:

CAN ARCHITECTURE- ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers- Application layers, Object layer, Transfer layer, Physical layer, Frame formats- Data frame, Remote frame, Error frame, Over load frame, Ack slot, Inter frame spacing, Bit spacing, Applications.

UNIT - III Lecture Hrs:

PCIe
Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration, Hardware and Software implementation, Hardware protocols, Applications.

UNIT - IV Lecture Hrs:

USB
Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, Isochronous transfer. Enumeration- Device detection, Default state, Addressed state, Configured state, enumeration sequencing. Descriptor types and contents- Device descriptor, configuration descriptor, Interface descriptor, Endpoint descriptor, String descriptor. Device driver.

UNIT - V Lecture Hrs:

Data streaming Serial Communication Protocal- Serial Front Panel Data Port(SFPDP) configurations, Flow control, serial FPDP transmission frames, fiber frames and copper cable.

Textbooks:

1. A Comprehensive Guide to controller Area Network – Wilfried Voss, Copperhill Media Corporation, 2nd Ed., 2005.
2.Serial Port Complete-COM Ports, USB Virtual Com Portsand Ports for Embedded Systems- Jan Axelson, Lakeview Research, 2nd Ed.,

Reference Books:

1. USB Complete – Jan Axelson, Penram Publications.
2.PCI Express Technology – Mike Jackson, Ravi Budruk, Mindshare Press.

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

Course Code	ROBOTICS	L	T	P	C
21D55301a		3	0	0	3
	Semester	III			

Course Objectives:

- To describe the various elements that make an industrial robot system
- To discuss various applications of industrial robot systems
- To analyze robot manipulators in terms of their kinematics, kinetics, and control
- To design a model robot manipulators and analyze their performance, through running simulations using a MATLAB-based Robot Toolbox

Course Outcomes (CO): Student will be able to

- Describe the various elements that make an industrial robot system
- Discuss various applications of industrial robot systems
- Analyze robot manipulators in terms of their kinematics, kinetics, and control
- Design a model robot manipulators and analyze their performance, through running simulations using a MATLAB-based Robot Toolbox

UNIT - I		Lecture Hrs:

Introduction & Basic Definitions: History pf robots-robot anatomy, Coordinate Systems , Human arm Characteristics , Cartesian , Cylindrical, Polar, coordinate frames , mapping transform.

UNIT - II		Lecture Hrs:

Kinematics – Inverse Kinematics: Kinematics , Mechanical structure and notations , description of links and joints , DenavitHatenberg notation , manipulator transformation matrix , examples inverse kinematics.

UNIT - III		Lecture Hrs:

Differential Motion – Statics – Dynamic Modeling: Velocity Propagation along links, manipulator Jacobian – Jacobian singularities – Lagrange Euler formulation Newton Euler formulation basics of trajectory planning.

UNIT - IV		Lecture Hrs:

Robot Systems : Actuators Sensors and Vision: Hydraulic and Electrical Systems Including Pumps, valves, solenoids, cylinders, stepper motors, Encoders and AC Motors Range and use of sensors, Microswitches, Resistance Transducers, Piezo-electric, Infrared and Lasers Applications of Sensors : Reed Switches, Ultrasonic, Barcode Readers and RFID – Fundamentals of Robotic vision.

UNIT - V		Lecture Hrs:

Robots and Applications.: Industrial Applications – Processing applications – Assembly applications, Inspection applications , Non Industrial applications.

Textbooks:

1. Robotics and Control : R.K. Mittal and I.J. Nagarath, TMH 2003.
2. Introduction to Robotics – P.J. Mckerrow, ISBN: 0201182408
3. Introduction to Robotics – S. Nikv, 2001, Prentice Hall,
4. Mechatronics and Robotics: Design & Applications – A. Mutanbara, 1999, CRC Press.

Reference Books:

1. Robotics – K.S. Fu, R.C. Gonzalez and C.S.G. Lee, 2008, TMH.

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M.TECH. IN EMBEDDED SYSTEMS

COURSE STRUCTURE & SYLLABI

AUDIT COURSE-I

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

Course Code	ENGLISH FOR RESEARCH PAPER WRITING	L	T	P	C
21DAC101a		2	0	0	0
	Semester	I			

Course Objectives: This course will enable students:

- Understand the essentials of writing skills and their level of readability
- Learn about what to write in each section
- Ensure qualitative presentation with linguistic accuracy

Course Outcomes (CO): Student will be able to

- Understand the significance of writing skills and the level of readability
- Analyze and write title, abstract, different sections in research paper
- Develop the skills needed while writing a research paper

UNIT - I	Lecture Hrs:10

1Overview of a Research Paper- Planning and Preparation- Word Order- Useful Phrases - Breaking up Long Sentences-Structuring Paragraphs and Sentences-Being Concise and Removing Redundancy -Avoiding Ambiguity

UNIT - II	Lecture Hrs:10

Essential Components of a Research Paper- Abstracts- Building Hypothesis-Research Problem - Highlight Findings- Hedging and Criticizing, Paraphrasing and Plagiarism, Cauterization

UNIT - III	Lecture Hrs:10

Introducing Review of the Literature – Methodology - Analysis of the Data-Findings - Discussion-Conclusions-Recommendations.

UNIT - IV	Lecture Hrs:9

Key skills needed for writing a Title, Abstract, and Introduction

UNIT - V	Lecture Hrs:9

Appropriate language to formulate Methodology, incorporate Results, put forth Arguments and draw Conclusions

Suggested Reading

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books) Model Curriculum of Engineering & Technology PG Courses [Volume-I]
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

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M.TECH. IN EMBEDDED SYSTEMS

COURSE STRUCTURE & SYLLABI

Course Code	DISASTER MANAGEMENT	L	T	P	C
21DAC101b		2	0	0	0
	Semester	I			

Course Objectives: This course will enable students:

- Learn to demonstrate critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluatedisasterriskreduction and humanitarian response policy and practice from Multiple perspectives.
- Developanunderstandingofstandardsofhumanitarianresponseandpracticalrelevanceinspecific types of disasters and conflict situations
- Criticallyunderstandthestrengthsandweaknessesofdisastermanagementapproaches,planningand programming in different countries, particularly their home country or the countries they work in

UNIT - I

Introduction:
Disaster:Definition,FactorsandSignificance;DifferenceBetweenHazardandDisaster;Naturaland Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:
Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post- Disaster Diseases and Epidemics

UNIT - II

Repercussions of Disasters and Hazards:
Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes,Volcanisms,Cyclones,Tsunamis,Floods,DroughtsandFamines,Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT - III

Disaster Preparedness and Management:
Preparedness: Monitoring of Phenomena Triggering ADisasteror Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT - IV

Risk Assessment Disaster Risk:
Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. TechniquesofRiskAssessment,GlobalCo-OperationinRiskAssessmentand Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT - V

Disaster Mitigation:
Meaning,ConceptandStrategiesofDisasterMitigation,EmergingTrendsInMitigation.Structural Mitigationand Non-Structural Mitigation, Programs of Disaster Mitigation in India.

Suggested Reading

1. R.Nishith,SinghAK,"DisasterManagementinIndia:Perspectives,issuesandstrategies
2. "'New Royal book Company..Sahni,PardeepEt.Al.(Eds.),"DisasterMitigationExperiencesAndReflections",PrenticeHall OfIndia, New Delhi.
3. GoelS.L.,DisasterAdministrationAndManagementTextAndCaseStudies",Deep&Deep Publication Pvt. Ltd., New Delhi

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M.TECH. IN EMBEDDED SYSTEMS

COURSE STRUCTURE & SYLLABI

Course Code	SANSKRITFOR TECHNICAL KNOWLEDGE	L	T	P	C
21DAC101c		2	0	0	0
	Semester	**I**			

Course Objectives: This course will enable students:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- LearningofSanskrittodevelopthelogicinmathematics,science&othersubjects enhancing the memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge
- Knowledge from ancientliterature

Course Outcomes (CO): Student will be able to

- Understanding basic Sanskrit language
- Ancient Sanskrit literature about science &technology can be understood
- Being a logical language will help to develop logic in students

UNIT - I		
Alphabets in Sanskrit,		
UNIT - II		
Past/Present/Future Tense, Simple Sentences		
UNIT - III		
Order, Introduction of roots		
UNIT - IV		
Technical information about Sanskrit Literature		
UNIT - V		
Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics		

Suggested Reading

1.“Abhyaspustakam” –Dr.Vishwas, Sanskrit-Bharti Publication, New Delhi
2.“Teach Yourself Sanskrit” Prathama Deeksha- VempatiKutumbshastri, RashtriyaSanskrit Sansthanam, New Delhi Publication
3.“India’s Glorious ScientificTradition” Suresh Soni, Ocean books (P) Ltd.,New Delhi

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M.TECH. IN EMBEDDED SYSTEMS
COURSE STRUCTURE & SYLLABI

AUDIT COURSE-II

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COURSE STRUCTURE & SYLLABI

Course Code	PEDAGOGY STUDIES	L	T	P	C
21DAC201a		2	0	0	0
	Semester	**II**			

Course Objectives: This course will enable students:

- Reviewexistingevidenceonthereviewtopictoinformprogrammedesignandpolicy making undertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

Course Outcomes (CO): Student will be able to

Students will be able to understand:

- Whatpedagogicalpracticesarebeingusedbyteachersinformalandinformalclassrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in what conditions, and with what population of learners?
- Howcanteachereducation(curriculumandpracticum)andtheschoolcurriculumand guidance materials best support effective pedagogy?

UNIT - I

Introduction and Methodology: Aims and rationale, Policy back ground, Conceptual frame work and terminology Theories oflearning,Curriculum,Teachereducation.Conceptualframework,Research questions**.** Overview of methodology and Searching.

UNIT - II

Thematic overview: Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

UNIT - III

Evidence on theeffectivenessofpedagogicalpractices,Methodologyfortheindepthstage:quality assessmen t of included studies. How can teacher education (curriculumandpracticum) andthescho curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of th body of evidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

UNIT - IV

Professional development: alignment with classroom practices and follow-up support, Peer support, Support from the head teacherandthecommunity.Curriculumandassessment,Barrierstolearning:limitedresourcesand large class sizes

UNIT - V

Researchgapsandfuturedirections: Researchdesign**,**Contexts**,**Pedagogy**,**Teachereducation**,** Curriculum and assessment**,** Dissemination and research impact.

Suggested Reading

1. AckersJ,HardmanF(2001)ClassroominteractioninKenyanprimaryschools,Compare, 31 (2): 245-261.
2. AgrawalM(2004)Curricularreforminschools:Theimportanceofevaluation,Journalof

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3. Curriculum Studies, 36 (3): 361-379.
4. AkyeampongK(2003) Teacher training in Ghana - does it count? Multi-site teachereducation research project (MUSTER) country report 1. London: DFID.
5. Akyeampong K, LussierK, PryorJ, Westbrook J (2013)Improving teaching and learning of basic maths and reading in Africa: Does teacherpreparation count?International Journal Educational Development, 33 (3): 272–282.
6. Alexander RJ(2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
   Chavan M (2003)ReadIndia: A mass scale, rapid, 'learning to read'campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

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COURSE STRUCTURE & SYLLABI

Course Code	**STRESSMANAGEMENT BY YOGA**	**L**	**T**	**P**	**C**
21DAC201b		**2**	**0**	**0**	**0**
	Semester	**II**			
Course Objectives: This course will enable students:					
• To achieve overall health of body and mind • To overcome stres					
Course Outcomes (CO): Student will be able to					
• Develop healthy mind in a healthy body thus improving social health also • Improve efficiency					
UNIT - I					
Definitions of Eight parts of yog.(Ashtanga)					
UNIT - II					
Yam and Niyam.					
UNIT - III					
Do`sand Don't'sin life. i) Ahinsa,satya,astheya,bramhacharyaand aparigrahaii) Shaucha,santosh,tapa,swadhyay,ishwarpranidhan					
UNIT - IV					
Asan and Pranayam					
UNIT - V					
i)Variousyogposesand theirbenefitsformind &body ii)Regularizationofbreathingtechniques and its effects-Types ofpranayam					
Suggested Reading					
1.'Yogic Asanas forGroupTarining-Part-I": Janardan SwamiYogabhyasiMandal, Nagpur 2."Rajayogaor conquering the Internal Nature" by Swami Vivekananda, Advaita Ashrama (Publication Department), Kolkata					

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COURSE STRUCTURE & SYLLABI

Course Code	PERSONALITY DEVELOPMENT THROUGHLIFE ENLIGHTENMENTSKILLS	L	T	P	C
21DAC201c		2	0	0	0
	Semester	**II**			

Course Objectives: This course will enable students:

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

Course Outcomes (CO): Student will be able to

- StudyofShrimad-Bhagwad-Geetawillhelpthestudentindevelopinghispersonalityand achieve the highest goal in life
- The person who has studied Geetawilllead the nation and mankind to peace and prosperity
- Study of Neetishatakam will help in developing versatile personality of students

UNIT - I

Neetisatakam- Holistic development of personality
Verses-19,20,21,22(wisdom)
Verses-29,31,32(pride &heroism)
Verses-26,28,63,65(virtue)

UNIT - II

Neetisatakam- Holistic development of personality
Verses-52,53,59(dont's)
Verses-71,73,75,78(do's)

UNIT - III

Approach to day to day work and duties.
ShrimadBhagwadGeeta:Chapter2-Verses41,47,48,
Chapter3-Verses13,21,27,35,Chapter6-Verses5,13,17,23,35,
Chapter18-Verses45,46,48.

UNIT - IV

Statements of basic knowledge.
ShrimadBhagwadGeeta:Chapter2-Verses 56,62,68
Chapter12 -Verses13,14,15,16,17,18
Personality of Rolemodel. Shrimad Bhagwad Geeta:

UNIT - V

Chapter2-Verses 17,Chapter3-Verses36,37,42,
Chapter4-Verses18,38,39
Chapter18– Verses37,38,63

Suggested Reading

1."SrimadBhagavadGita"bySwamiSwarupanandaAdvaitaAshram(PublicationDepartment), Kolkata
2.Bhartrihari'sThree Satakam (Niti-sringar-vairagya) by P.Gopinath, RashtriyaSanskrit Sansthanam, New Delhi.

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OPEN ELECTIVE

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COURSE STRUCTURE & SYLLABI

Course Code	INDUSTRIAL SAFETY	L	T	P	C
21DOE301b		3	0	0	3
Semester		III			

Course Objectives:

- To know about Industrial safety programs and toxicology, Industrial laws , regulations and source models
- To understand about fire and explosion, preventive methods, relief and its sizing methods
- To analyse industrial hazards and its risk assessment.

Course Outcomes (CO): Student will be able to

- To list out important legislations related to health, Safety and Environment.
- To list out requirements mentioned in factories act for the prevention of accidents.
- To understand the health and welfare provisions given in factories act.

UNIT - I Lecture Hrs:

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT - II Lecture Hrs:

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT - III Lecture Hrs:

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working andapplications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT - IV Lecture Hrs:

Fault tracing: Fault tracing-concept and importance, decision treeconcept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic,automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT - V Lecture Hrs:

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Textbooks:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.

Reference Books:

1. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
2. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

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COURSE STRUCTURE & SYLLABI

Course Code	BUSINESS ANALYTICS	L	T	P	C
21DOE301c		3	0	0	3
Semester		III			

Course Objectives:

- The main objective of this course is to give the student a comprehensive understanding of business analytics methods.

Course Outcomes (CO): Student will be able to

- Students will demonstrate knowledge of data analytics.
- Students will demonstrate the ability of think critically in making decisions based on data and deep analytics.
- Students will demonstrate the ability to use technical skills in predicative and prescriptive modeling to support business decision-making.
- Students will demonstrate the ability to translate data into clear, actionable insights.

UNIT - I — Lecture Hrs:

Business Analysis: Overview of Business Analysis, Overview of Requirements, Role of the Business Analyst.
Stakeholders: the project team, management, and the front line, Handling Stakeholder Conflicts.

UNIT - II — Lecture Hrs:

Life Cycles: Systems Development Life Cycles, Project Life Cycles, Product Life Cycles, Requirement Life Cycles.

UNIT - III — Lecture Hrs:

Forming Requirements: Overview of Requirements, Attributes of Good Requirements, Types of Requirements, Requirement Sources, Gathering Requirements from Stakeholders, Common Requirements Documents.Transforming Requirements: Stakeholder Needs Analysis, Decomposition Analysis, Additive/Subtractive Analysis, Gap Analysis, Notations (UML & BPMN), Flowcharts, Swim Lane Flowcharts, Entity-Relationship Diagrams, State-Transition Diagrams, Data Flow Diagrams, Use Case Modeling, Business Process Modeling

UNIT - IV — Lecture Hrs:

Finalizing Requirements: Presenting Requirements, Socializing Requirements and Gaining Acceptance, Prioritizing Requirements. Managing Requirements Assets: Change Control, Requirements Tools

UNIT - V — Lecture Hrs:

Recent Trands in: Embedded and colleborative business intelligence, Visual data recovery, Data Storytelling and Data Journalism.

Textbooks:

1. Business Analysis by James Cadle et al.
2. Project Management: The Managerial Process by Erik Larson and, Clifford Gray

Reference Books:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education.

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COURSE STRUCTURE & SYLLABI

Course Code	**WASTE TO ENERGY**	**L**	**T**	**P**	**C**
21DOE301e		**3**	**0**	**0**	**3**
	Semester	**III**			

Course Objectives:

- Introduce and explain energy from waste, classification and devices to convert waste to energy.
- To impart knowledge on biomass pyrolysis, gasification, combustion and conversion process.
- To educate on biogas properties ,bio energy system, biomass resources and their classification and biomass energy programme in India.

Course Outcomes (CO): Student will be able to

- To know about overview of Energy to waste and classification of waste.
- To acquire knowledge on bio mass pyrolysis, gasification, combustion and conversion process in detail.
- To gain knowledge on properties of biogas, biomass resources and programmes to convert waste to energy in India.

UNIT - I	Lecture Hrs:10

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

UNIT - II	Lecture Hrs:10

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT - III	Lecture Hrs:12

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation

UNIT - IV	Lecture Hrs:12

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT - V	Lecture Hrs:10

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification -
Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification- pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

Textbooks:

1. Non Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 2018
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., TMH, 2017

Reference Books:

1. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
2. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996

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Online Learning Resources:
https://nptel.ac.in/noc/courses/noc19/SEM1/noc19-ch13/ https://www.youtube.com/watch?v=x2KmjbCvKTk